REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-23 in the application. In previous responses, the Applicant amended Claims 1, 9 and 17, canceled Claims 5, 13 and 21 and added new Claims 24-26. In the present response, the Applicant has amended Claims 1-3, 6-11, 14-15, 17-19 and 22-26. Accordingly, Claims 1-4, 6-12, 14-20 and 22-26 are currently pending in the application.

I. Rejection of Claims 1-4, 6-12, 14-20 and 22-26 under 35 U.S.C. §112

The Examiner has rejected Claims 1-4, 6-12, 14-20 and 22-26 under 35 U.S.C. §112, ¶1, for failing to comply with the enablement requirement. More specifically, the Examiner has asserted that the specification does not describe how to use a mispredict PC queue in conjunction with staging registers. (*See* Examiner's Action, page 2.) The Applicants respectfully disagree.

The Applicant directs the Examiner to Figures 3 and 4 and the corresponding discussion in paragraphs 55 and 57 on pages 22 to 24 of the specification. A mispredict PC value, corresponding to a branch not predicted to be the outcome of a conditional branch, is generated and stored in the mispredict PC FIFO queue 234 for possible later use. The staging registers 340 allow the mispredict PC value to be drawn from the mispredict PC FIFO 234 and to track its corresponding conditional branch instruction as it moves through stages in a pipeline. (*See* paragraph 55, page 22 and Figure 3.) When the conditional branch instruction corresponding to the mispredict PC value contained in one of the slots of the mispredict PC FIFO queue 234 actually enters the pipeline, that slot is selected by way of the multiplexer 420, causing the mispredict PC value to move into the staging registers 340. As the corresponding conditional branch instruction moves through the various stages of the pipeline, the mispredict PC value moves through the corresponding staging registers 340. (*See*

paragraph 57, pages 23-24.) Thus, the specification sufficiently enables one skilled in the art to utilize a mispredict PC queue with staging registers. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §112, ¶1, rejection of Claims 1-4, 6-12, 14-20 and 22-26 and allow issuance thereof.

II. Rejection of Claims 1-4, 6-12, 14-20 and 22-26 under 35 U.S.C. §112, ¶2

The Examiner has rejected Claims 1-4, 6-12, 14-20 and 22-26 under35 U.S.C. §112, ¶2, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. The Applicant respectfully disagrees since independent Claims 1, 9 and 17 have been amended rendering this rejection moot. Additionally, as explained above in response to the §112, ¶1, rejection, the Applicant has pointed out the interaction and operation of the mispredict PC queue and the staging registers. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §112, ¶2, rejection of Claims 1-4, 6-12, 14-20 and 22-26 and allow issuance thereof.

III. Rejection of Claims 1-4, 6-12, 14-20 and 22-26 under 35 U.S.C. §102

The Examiner rejected Claims 1-4, 6-12, 14-20 and 22-26 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,578,134 to Van Dyke, *et al*. The Applicant respectfully disagrees.

Van Dyke does not teach reducing pipeline stalls between conditional branches as recited in independent Claims 1, 9 and 17. More specifically, Van Dyke does not teach selecting one of multiple mispredict PC values to track a corresponding conditional branch instruction as the

corresponding conditional branch instruction moves through stages of the pipeline wherein the selecting is based on when the corresponding conditional branch instruction enters the pipeline as recited in independent Claims 1, 9 and 17. On the contrary, the Applicant does not find any teaching in Van Dyke of selecting a mispredict PC value for tracking a conditional branch instruction. Instead, Van Dyke teaches sending a target PC down an alternate PC 34 if a prediction is not taken and sending the next sequential address to the instruction cache. (*See* column 8, lines 51-63 and Figure 3.) Thus, Van Dyke teaches sending a next sequential value to the instruction cache when a mispredict occurs but provides no teaching of selecting a mispredict PC value to track a conditional branch instruction as recited in independent Claims 1, 9 and 17.

Since Van Dyke does not disclose each and every element of independent Claims 1, 9 and 17, Van Dyke does not anticipate Claims 1, 9 and 17 and Claims dependent thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to Claims 1-4, 6-12, 14-20 and 22-26.

IV. Rejection of Claims 1-4, 6-12, 14-20 and 22-26 under 35 U.S.C. §102

The Examiner rejected Claims 1-4, 6-12, 14-20 and 22-26 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,933,850 to Kumar, *et al.* The Applicant respectfully disagrees.

Kumar does not teach reducing pipeline stalls between conditional branches as recited in independent Claims 1, 9 and 17. More specifically, Kumar does not teach selecting one of multiple mispredict PC values to track a corresponding conditional branch instruction as the corresponding conditional branch instruction moves through stages of the pipeline wherein the selecting is based

on when the corresponding conditional branch instruction enters the pipeline as recited in independent Claims 1, 9 and 17. Instead, as illustrated in one embodiment, Kumar teaches supplying a misprediction address through an alternate address pipeline. Addresses are input into the alternate address pipeline via a multiplexer which selects one of a sequential address and a target address based on an interrupt signal and a branch with prediction signal. (*See* column 6, lines 33-59 and Figure 5.) Thus, Kumar does not select a mispredict PC value from multiple mispredict PC values but teaches supplying a misprediction address from a sequential address and a target address. Additionally, Kumar does not select a mispredict PC value based on when a corresponding conditional branch instruction enters a pipeline but based on an interrupt signal and a branch with prediction signal. Thus, Kumar provides no teaching of selecting a mispredict PC value to track a conditional branch instruction as recited in independent Claims 1, 9 and 17.

Since Kumar does not disclose each and every element of independent Claims 1, 9 and 17, Kumar does not anticipate Claims 1, 9 and 17 and Claims dependent thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to Claims 1-4, 6-12, 14-20 and 22-26.

V. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-4, 6-12, 14-20 and 22-26.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES, PC

J. Joel Justiss
Registration No. 48,981

Dated: 4/18/05

P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800